

FIG._3

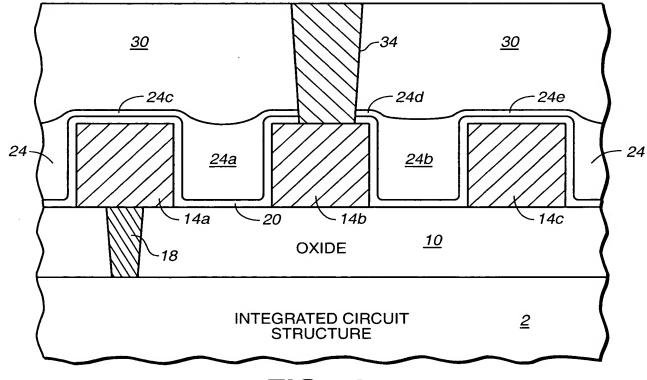
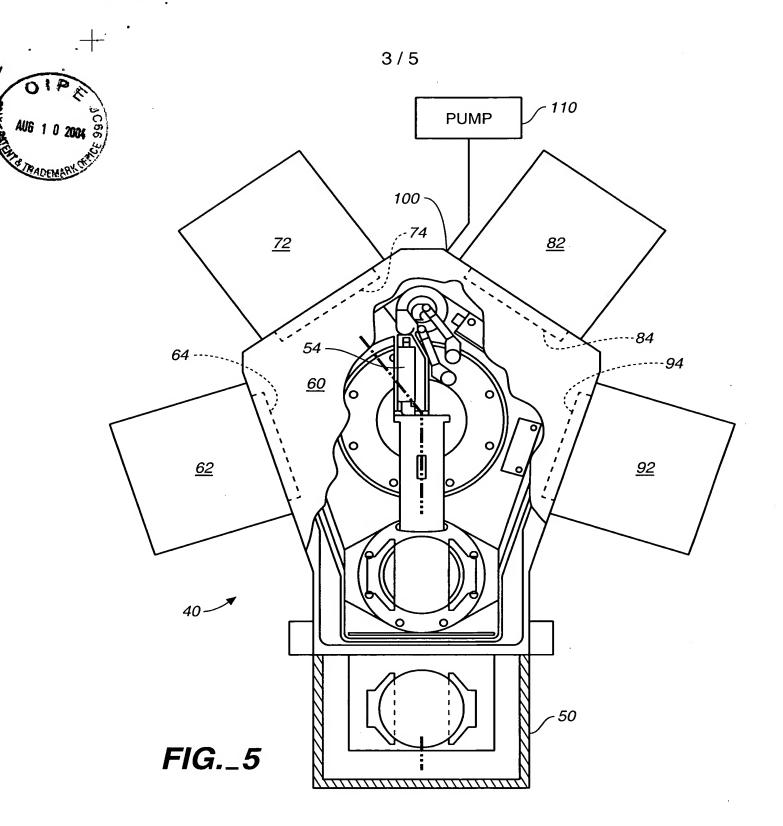


FIG._4

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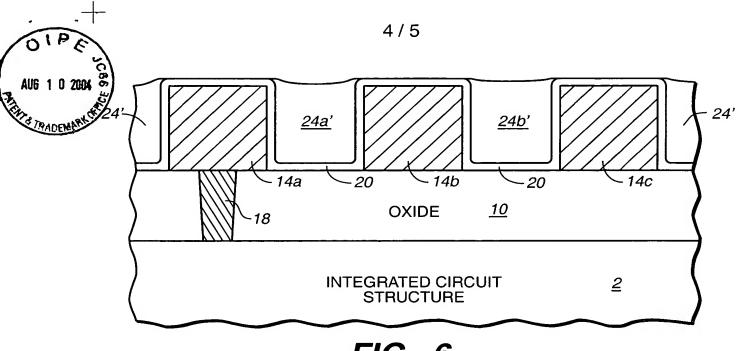


FIG._6

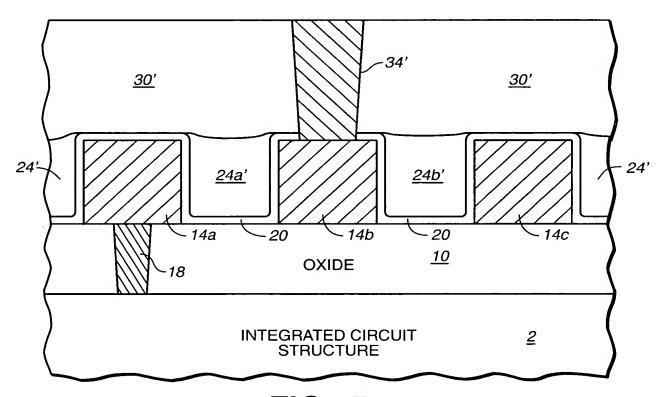


FIG._7

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FORMING CLOSELY SPACED APART METAL LINES ON AN OXIDE LAYER OF AN INTEGRATED CIRCUIT STRUCTURE ON A SEMICONDUCTOR SUBSTRATE

DEPOSITING A THIN CONFORMAL BASE LAYER OF DIELECTRIC MATERIAL OVER THE METAL LINES AND THE OXIDE LAYER IN A VACUUM DEPOSITION APPARATUS

FORMING IN THE SAME VACUUM DEPOSITION APPARATUS A FIRST LAYER OF LOW K DIELECTRIC MATERIAL OVER THE STRUCTURE UP TO AT LEAST THE LEVEL OF THE TOP OF THE METAL LINES USING A LOW K SILICON OXIDE DIELECTRIC MATERIAL CAPABLE OF FILLING HIGH ASPECT RATIO REGIONS BETWEEN CLOSELY SPACED APART METAL LINES WITHOUT FORMING VOIDS

DEPOSITING IN THE SAME VACUUM
DEPOSITION APPARATUS A SECOND LAYER
OF LOW K DIELECTRIC MATERIAL OVER
THE FIRST LAYER OF LOW K DIELECTRIC
MATERIAL USING A PROCESS WHICH WILL
DEPOSIT LOW K DIELECTRIC MATERIAL AT
A RATE COMPARABLE TO DEPOSITION
OF STANDARD K DIELECTRIC MATERIAL

FIG._8